Carleton University
Dept. of Systems and Computer Engineering

Computer Organization—SYSC 3006 Fall 2017

Course Outline

Instructor  Dr. Ramy Gohary, Office: ME4474, T. 613-520-2600 Ext. 5595, Email: gohary@sce.carleton.ca, Office hours: Monday and Friday 1:30–3:00.

Teaching Assistants

• TBD

Course Description  This is a first course on the organization of computer systems at the hardware/software interface. Understanding this interface involves the processor’s Instruction Set Architecture (ISA), the system’s memory organization, and the system’s I/O peripherals. Engineers working with microcontrollers (including mobile devices) must understand computer systems at this level, and these concepts form the foundation on which more powerful computer systems are based (such as desktop systems, servers, multiprocessors, and supercomputers).

The processor’s native assembly language is a central software topic in the course. The increasing use of high level languages such as C is reducing the need for assembly language programming proficiency. As a result, the course will focus more on understanding how an assembly language manipulates information at the hardware/software interface and can support a high level language, and will not emphasize developing complete applications in assembly language.


Prerequisites  (SYSC-2002 or SYSC-2006) and ELEC-2607. This course precludes additional credit for SYSC-2001 and SYSC-2003. This course may not be taken for credit by students in Computer Systems Engineering, Communications Engineering, or Software Engineering.

Students who have not satisfied the prerequisites for this course must either a) withdraw from the course, or b) obtain a prerequisite waiver online at http://www.carleton.ca/engineering-design/current-students/undergrad-academic-support/, or c) will be deregistered from the course after the last day to register for courses.

Website  The course will use the SYSC3006A (LEC) Fall 2016 website on cuLearn. Course materials will be placed on the website for student personal use, and students are responsible for checking the website frequently. Student, TA or professor materials created for this course (including presentations and posted notes, labs, case studies, assignments and exams) remain the intellectual property of the author(s). They are intended for personal use and may not be reproduced or redistributed without prior written consent of the author(s).
Textbooks A specific textbook is not recommended in the course. Course notes and supporting material will be supplied via the course webpage for student personal use.

Attendance Students are expected to attend all lectures and labs. The Faculty of Engineering and Design requires its students to have a conflict-free timetable, so requests to accommodate missed exams, assignment due dates, etc., because of conflicts with other courses, jobs or vacation plans will not be considered.

Laboratory There will be 10 graded laboratories that will be posted on the course website. The first session of Lab 1 is on Monday, Sept. 12. Lab attendance is mandatory, with work to be demonstrated by the end of the lab period. Marks will only be awarded for labs demonstrated during the students schedule lab time (according to section registration). During the scheduled lab times, TA assistance will be available. The computer lab is open seven days a week, whenever the building is open. You may use the lab at any time other than those timeslots when the lab is reserved for other courses or for other sections of this course.

Study Questions Study questions will be posted on the course website, but will not be collected and graded.

Students are encouraged to discuss issues when working on labs; however, they are expected to do their own lab work individually. Suspected plagiarism will be investigated and may result in a mark of zero for the lab. As well, alleged instructional offences will be reported to the Associate Dean of Engineering. (Please see the current undergraduate calendar, “Instructional Offences”, in the Undergraduate Calendar Supplement).

Students are warned that the labs and study questions form a very important part of this course doing these (by yourself) is an excellent way for you to learn the material. In this context, it should be noted that copying labs is, even if you are not caught, a self-defeating exercise. Historically, most of the students who resorted to copying did not do particularly well on the mid-term or final exam.

Quizzes Students will be expected to participate in in-class discussions and to write 5-minute quizzes. Quiz times will be announced beforehand as the course progresses.

Midterm Exam There will be one closed book, no-calculator, midterm test. The midterm test will be held at 6:00 PM on Friday October 20, 2017 in room TBD.

Final Exam A closed book, no-calculator, final exam will be held during the University’s formal examination period.

Students who miss the final exam may be granted permission to write a deferred examination (see the Undergraduate Calendar for regulations on deferred exams).

Grading Scheme

- Labs: 20%
- Quizzes: 10%
- Mid-term test: 25%
- Final exam: 45%

Medical Certificates A medical certificate must adhere to the format required by the Registrar. The format is available as a PDF form through the Registrar’s website http://www.carleton.ca/registrar/forms. All medical certificates must be presented immediately upon return from the illness; they will not be accepted after the fact.
**Academic accommodation for religious obligations**  Students who require accommodations due to religious obligations must follow the procedures described in Section 2.10 of the “Academic Regulations of the University”.

**Students with Disabilities**  Students with disabilities requiring academic accommodations in this course should contact the Paul Menton Centre for Students with Disabilities (PMC) (UC 500) to complete the necessary forms. After registering with the PMC, make an appointment with your instructor to discuss your specific needs at least two weeks prior to the mid-term exam. This will allow sufficient time to make the required arrangements.

The Paul Menton Centre for Students with Disabilities (PMC) provides services to students with Learning Disabilities (LD), psychiatric/mental health disabilities, Attention Deficit Hyperactivity Disorder (ADHD), Autism Spectrum Disorders (ASD), chronic medical conditions, and impairments in mobility, hearing, and vision. If you have a disability requiring academic accommodations in this course, please contact PMC at 613-520-6608 or pmc@carleton.ca for a formal evaluation. If you are already registered with the PMC, contact your PMC coordinator to send me your Letter of Accommodation at the beginning of the term, and no later than two weeks before the first in-class scheduled test or exam requiring accommodation (if applicable). Requests made within two weeks will be reviewed on a case-by-case basis. After requesting accommodation from PMC, meet with me to ensure accommodation arrangements are made. Please consult the PMC website (www.carleton.ca/pmc) for the deadline to request accommodations for the formally-scheduled exam (if applicable).

**Lecture Content**  The following themes are interwoven in the lectures throughout the course.

- **Introduction to FPGA and Verilog HDL**
- **Computer system architecture (basics)**
  - Computer system components: processor, memory, I/O, interconnection bus
  - Information encoding, data representation in binary, hexadecimal
  - Number systems, unsigned integers, signed integers, 2’s complement
  - Computer hardware organization: datapath and control
  - Registers, instruction cycle
- **Hardware/software interface (Instruction Set Architecture)**
  - Instructions: data manipulation, data transfer, control flow, instruction encoding
  - Computer arithmetic, flags
- **Microcontroller example**
  - Microcontroller concept
  - System on Chip, memory model, ISA
- **Assembly language programming**
  - Code snippets, examples
  - Assembly process, linker, loader
- **High-level Language Support**
  - Variables, arrays, structures, assignment, looping, conditional statements
  - Procedures and functions, parameter passing
Peripheral I/O and Interrupts

- Register model of peripheral devices: parallel I/O, serial I/O, timers
- Polling
- Hardware interrupts: vectored and prioritized, Nested Vector Interrupt Controller (NVIC)
- Examples: timer, serial
- Software interrupts, o/s calls